## REMARKS

Claims 1-19 and 21-30 are pending in this application. By this Amendment, claims 1, 8, 15, 19, 21, and 28 are amended. The amendments are supported by the specification at least at Figs. 4 and 5. No new matter is added.

### I.    Rejection of Claims Under 35 U.S.C. §103

The Office Action rejects claims 1-11, 14-18, and 28-30 under 35 U.S.C. §103(a) over Narasimhan (U.S. Patent No. 6,446,192) in view of Bishop (U.S. Patent No. 4,914,653); and claims 12, 13, 19, and 21-27 under 35 U.S.C. §103(a) over Narasimhan in view of Bishop and further in view of Balachandran (U.S. Patent Application Publication No. 2005/0078620). Applicant respectfully traverses this rejection.

Applicant respectfully submits that Narasimhan, Bishop, and Balachandran, either alone or combined, do not disclose or render obvious at least access for allowing another microprocessor subsystem to perform a management function even when the processor core is not responsive to any signal, as recited in independent claim 1, and similarly recited in independent claims 8, 15, 19, and 28.

Specifically, the Office Action, on page 3, asserts that the Direct Memory Access (DMA) disclosed by Narasimhan (alleged management control block) can perform data transfer function (alleged management function) without a CPU or microcontrollers (alleged processor core), and thus obviates requiring responsive processor cores on the device. However, as explained during the interview, it is well known in the art that a DMA (also synonymous to DMAC) has to interact with a processor at least at the beginning and ending of the DMA's operation: "[w]hen the DMAC needs to initiate a bus operation, it *must first request control* of the bus by asserting BR [bus request]. The processor *responds* by completing its current bus operation and then asserting

-14-

BG [bus grant]. DMAC then becomes the bus master. The processor will not attempt to initiate another bus operation until BR is released. DMAC releases BR [to the processor] when it is finished using the bus for the moment, and the processor again becomes the bus master." See Leonard R. Marino, *Principles of Computer Design* 13 (Alfred V. Aho et al. eds., Computer Science Press 1991)(1986).

In other words, the CPU must be *responsive* to the DMA's bus request to perform data transfer operation at least from the beginning of the data transfer operation. The DMA is only designed to perform the data transfer operation on behalf of the CPU temporarily so that the CPU can perform other non-bus operations while the data transfer is in progress by the DMA. Then, the CPU receives an interrupt from the DMA controller (DMAC) once the data transfer operation is completed. Thus, the DMA cannot start to operate when the CPU or microcontrollers are not responsive to signals from the DMA. Therefore, the DMA does not obviate requiring responsive processor cores on the device.

The Advisory Action introduces a new ground of rejection based on Narasimhan's disclosures at col. 2 and lines 50-55, which was not raised by the June 18, 2009 Office Action. The Advisory Action asserts that the Narasimhan's disclosures teaches the above-noted feature. Applicant respectfully disagrees with this assertion as explained below.

Specifically, Narasimhan states, "[r]emarkably, this single network interface chip (NIC) provides all the networking hardware, networking software and device interface elements necessary for network connectivity and web-based or network-based management of any device. It [the single network interface chip] also enables monitoring and controlling of any device, regardless of its available processing power, code space, or interface pins. Even devices without

-15-

a CPU or microcontroller are supported [by the single network interface chip]" (see col. 2 and lines 50-55 of Narasimhan).

The above disclosures of Narasimhan does not teach that the NIC (alleged management port) can access for allowing another microprocessor subsystem to perform a management function even when the processor core is not responsive to any signal. The NIC's ability to enable monitoring and controlling of any device, regardless of the NIC's available processing power does not imply that the NIC can enable monitoring and controlling of any device even when its processor core or its CPU is not responsive to any signal.

As explained above with DMA, the CPU must be *responsive* to the DMA for the DMA to perform data transfer operation while the CPU has no processing power available for performing the data transfer operation. Thus, having limited processing power available in the CPU does not necessarily mean that the CPU does not need to be responsive to any signal. Thus, Narasimhan does not disclose performing a management function even when the processor core is not responsive to any signal.

Moreover, Narasimhan's statement, "[e]ven devices without a CPU or microcontroller are supported," means that the NIC can support *other* devices without a CPU or microcontroller. The Advisory Action's statement "Narasimhan Col. 2 Lines 50-55 disclosed performing management commands . . . using the device bus even without a CPU or microcontrollers" is a misinterpretation of the above-noted sentence. Narasimhan does not teach that the NIC can perform the management function even without a CPU or microcontroller; Narasimhan only teaches that the NIC can support other devices without a CPU or microcontroller.

In view of the above, Narasimhan does not disclose or render obvious at least access for allowing another microprocessor subsystem to perform a management function even when the processor core is not responsive to any signal, as recited in claim 1, and similarly recited in claims 8, 15, 19, and 28. Further, Bishop and Balachandran, either alone or combined, do not disclose or render obvious at least this feature.

Therefore, Applicant respectfully asserts that independent claims 1, 8, 15, 19, and 28 are allowable. Claims 2-7 depend from claim 1; claims 9-14 depend from claim 8, claims 16-18 depend from claim 15, claims 21-27 depend from claim 19, and claims 29 and 30 depend from claim 28. Claims 2-7, 9-14, 16-18, 21-27, 29, and 30 are therefore also allowable by virtue of their dependence, as well as for the additional features that they recite. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-19 and 21-30 under 35 U.S.C. §103(a).

## II.   Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-19 and 21-30 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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Attachments: Request for Continued Examination (RCE)
Petition for Extension of Time

Date: October 19, 2009

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